Claims

What is claimed is:

[c1] An integrated circuit having a top metal layer, the top metal layer having a first metal bar and a second metal bar, the integrated circuit comprising:

a first bump disposed on the first metal bar;

a second bump disposed on the first metal bar; and

a reference bump disposed on the second metal bar,

wherein the first bump and the second bump are positioned such that an angle between a line from the reference bump to the first bump and a line from the reference bump to the second bump has a value substantially equal to 150 degrees.

[c2] The integrated circuit of claim 1, wherein the first bump, the second bump, and the reference bump form a bump structure that is repeated across the top metal layer to form a patterned bump array.

[c3] The integrated circuit of claim 1, wherein the first bump, the second bump, and the reference bump for a bump structure that is repeated across a portion of the top metal layer.

[c4] The integrated circuit of claim 1, wherein the first metal bar is operatively connected to a voltage source, and wherein the second metal bar is operatively connected to ground.

[c5] The integrated circuit of claim 1, wherein the value of the angle is dependent on at least one selected from the group consisting of: a desired capacitance, a desired resistance, a desired inductance, a desired bump current flow, a desired bump population on the top metal layer, and desired signal track availability.

[c6] An integrated circuit having a top metal layer, the top metal layer having a first metal bar and a second metal bar, the integrated circuit comprising:

a first bump disposed on the first metal bar;

a second bump disposed on the first metal bar; and

a reference bump disposed on the second metal bar,

wherein the first metal bar and the second metal bar are positioned such that

an angle between a line from the reference bump to the first bump and a line from the reference bump to the second bump has a value substantially equal to 150 degrees.

[c7] The integrated circuit of claim 6, wherein the first bump, the second bump, and the reference bump form a bump structure that is repeated across the top metal layer to form a patterned bump array.

[c8] The integrated circuit of claim 6, wherein the first bump, the second bump, and the reference bump for a bump structure that is repeated across a portion of the top metal layer.

[c9] The integrated circuit of claim 6, wherein the first metal bar is operatively connected to a voltage source, and wherein the second metal bar is operatively connected to ground.

[c10] The integrated circuit of claim 6, wherein the value of the angle is dependent on at least one selected from the group consisting of: a desired capacitance, a desired resistance, a desired inductance, a desired bump current flow, a desired bump population on the top metal layer, and desired signal track availability.

[c11] A patterned bump array for a power grid of an integrated circuit, comprising:

a reference bump disposed on a first metal bar;

a first bump disposed on a second metal bar; and

a second bump disposed on a second metal bar,

wherein the first bump, the second bump, and the reference bump are arranged such that an angle between a line from the reference bump to the first bump and a line from the reference bump to the second bump has a value substantially equal to 150 degrees.

[c12] The patterned bump array of claim 11, wherein the first metal bar and second metal bar form a portion of the power grid.

[c13] The patterned bump array of claim 11, wherein the first metal bar is operatively connected to power, and wherein the second metal bar is operatively connected to ground.

[c14] The patterned bump array of claim 11, wherein the arrangement of the first bump, the second bump, and the reference bump is repeated across the power grid.

[c15] The patterned bump array of claim 11, wherein the arrangement of the first bump, the second bump, and the reference bump is repeated across a portion of the power grid.

[c16] The patterned bump array of claim 11, wherein the value of the angle is dependent on at least one selected from the group consisting of: a desired capacitance, a desired resistance, a desired inductance, a desired bump current flow, a desired bump population on the top metal layer, and desired signal track availability.

[c17] A bump layout for a power grid of an integrated circuit, comprising:

a reference bump disposed on a first metal bar;

a first bump disposed on a second metal bar; and

a second bump disposed on a second metal bar,

wherein the first metal bar and the second metal bar are arranged such that an angle between a line from the reference bump to the first bump

and a line from the reference bump to the second bump has a value substantially equal to 150 degrees.

[c18] The bump layout of claim 17, wherein the first metal bar and second metal bar form a portion of the power grid.

[c19] The bump layout of claim 17, wherein the first metal bar is operatively connected to power, and wherein the second metal bar is operatively connected to ground.

[c20] The bump layout of claim 17, wherein the arrangement of the first metal bar and the second metal bar is repeated across the power grid.

[c21] The bump layout of claim 17, wherein the arrangement of the first metal bar and the second metal bar is repeated across a portion of the power grid.

[c22] The bump layout of claim 17, wherein the value of the angle is dependent on at least one selected from the group consisting of: a desired capacitance, a desired resistance, a desired inductance, a desired bump current flow, a desired bump population on the top metal layer, and desired signal track availability.